REMARKS

Claims 1 to 18 are now pending and being considered.

It is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

Applicants thank the Examiner for accepting the Drawings, for acknowledging and considering the previously filed IDS and 1449 papers, and for acknowledging the priority claim and receipt of the priority documents.

With respect to paragraphs five (5) and six (6) of the Office Action, Applicants thank the Examiner for allowing claims 8 to 11, and for indicating that claims 5, 6, 7, and 12 to 17 contain allowable subject matter and would be allowed if rewritten to include the features of their respective base claims. As to the objections to claims 5, 6, 7, and 12 to 17, the objections are traversed since, as explained below, the base claims are allowable. It is therefore respectfully requested that the objections be withdrawn.

With respect to paragraph one (1), claim 2 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite because L was assertedly not defined. While the rejection may not be agreed with, to facilitate matters, claim 2 has been rewritten. It is therefore respectfully requested that the indefiniteness rejection of claim 2 be withdrawn.

With respect to paragraph two (2) of the Office Action, claims 1 and 18 were rejected under 35 U.S.C. § 102(b) as anticipated by "Okamoto", U.S. Patent No. 5,703,511.

As regards the anticipation rejections of the claims, to reject a claim under 35 U.S.C. § 102, the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. (See *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991)). Still further, not only must each of the claim features be identically described, an anticipatory reference must also enable a person having ordinary skill in the art to practice the claimed subject matter, as discussed herein. (See *Akzo, N.V. v. U.S.I.T.C.*, 1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986)).

As further regards the anticipation rejections, to the extent that the Office Action may be relying on the inherency doctrine, it is respectfully submitted that to rely on inherency, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; and see *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Int'f. 1990)). Thus, the M.P.E.P. and the case law make clear that simply because a certain result or characteristic may occur in the prior art

does not establish the inherency of that result or characteristic. Accordingly, it is respectfully submitted that any anticipation rejection premised on the inherency doctrine must fail absent the foregoing conditions.

Claim 1 is to a clock/data recovery circuit including: a voltage control oscillator for generating a clock signal of a frequency of 1/K (K=2,3,···) of a bit rate *of an input data signal*; *a delay circuit for delaying said input data signal for timing adjustment*; *a demultiplexer for demultiplexing said input data signal into M demultiplexed signals (M=2,3,···) by using said clock signal; a multiplexer for multiplexing said M demultiplexed signals by using said clock signal; a phase comparator for comparing phases of an output signal of said delay circuit and an output signal of said multiplexer*; a lowpass filter for extracting DC voltage from an output signal of said phase comparator and for inputting said DC voltage to said voltage control oscillator as a control voltage; in which *said clock/data recovery circuit outputs said clock signal generated by said voltage control oscillator as a recovery divided clock signal, and outputs said M demultiplexed signals from said demultiplexer as recovery parallel data signals.*

Claim 18 includes features like those of claim 1.

The Office Action essentially asserts that claims 1 and 18 are identically disclosed by Figures 19 and 20 of the Okamoto reference. Figure 19 in Okamoto refers to a fiber-channel transceiver IC, and Figure 20 refers to the clock generator 62 of Figure 19. The Office Action equates "labels 625, 626 and 626" with the VCO of the claimed subject matter. But, this portion does not identically describe (or even suggest) the feature of generating a clock signal of a frequency of 1/K (K=2,3,···) of a bit rate of an input data signal. Figure 20 (clock generator 62) does not identically describe or in any way suggest anything about an input data signal.

The Office Action equates label 621 with the delay circuit of the claimed subject matter. However, the label 621 delays reference clock but does not delay an input data signal (that is to be demultiplexed). The Office Action equates DEMUX 64 and MUX 61 with the demultiplexer and multiplexer of the claimed subject matter. But, DEMUX 64 and MUX 61 respectively do not operate using the clock signal of a frequency of 1/K (K=2, 3,···) of a bit rate of an input data signal, as provided for in the context of the claimed subject matter The clock output from the clock generator 62 is 1GHz -- which is not 1/K of any data. In addition, Figure 19 does not identically describe (or even suggest) that MUX 61 multiplexes data output from DEMUX 64.

Still further, the Office Action equates label 622 with the phase comparator of the claimed subject matter, but the label 622 does not compare an output signal or the MUX 61 with any data, as provided for in the context of the claimed subject matter.

Accordingly, claims 1 and 18 are allowable for the foregoing reasons, as are the dependent claims 2 to 7 and 12 to 17, which depend from claim 1.

As further regards claim 3, which depends from claim 1, Figure 21 refers to a clock recovery circuit of the circuit of Figure 19. The Office Action equates labels 631 and 630 with the another delay circuit of the claimed subject matter, but labels 631 and 630 are not provided before the delay circuit as provided for in the context of claim 1. The Office Action equates labels 631 and 632 with the another phase comparator of the claimed subject matter, but labels 631 and 632 do not compare the output data from the MUX with any data, as provided for in the context of the claimed subject matter.

With further respect to claim 4, claim 4 is allowable since claim 1 is allowable (and since the secondary "Obana" reference does not suggest these features of claim 1, as explained below). In addition, "Obana" does not disclose or suggest the feature of claim 4. For example, "Obana" does not disclose or suggest the second D-type ms-flip flop circuit for receiving said input data signal by using an inverted signal of said clock signal, and also does not disclose or suggest the claimed selector for selecting alternately an output signal of said first D-type ms-flip flop circuit and an output signal of said second D-type ms-flip flop circuit. Accordingly, claim 4 is allowable for this further reason.

Still further as to the presently claimed subject matter of claims 1 and 18, and as explained at page 4, line 29 to page 5, line 5 and Fig. 4, and at page 43, line 7 to page 44, page 32 of the present application, according to a "conventional" CDR that includes a decision circuit (DFF) which receives an input data signal and an VCO output signal having the same oscillation frequency as the input data bit rate, the VCO requires very high speed, so that the operation becomes unstable and power consumption is large. For solving this problem, according to the presently claimed subject matter, the DEMUX-MUX structure is adopted as the decision circuit for enabling data deciding operation at a low clock speed – i.e., 1/K of input data bit rate. That is, the input data signal is demultiplexed into parallel signals by the DEMUX according to the 1/K clock signal. By this operation, the phase of

each parallel signal is synchronized with the 1/K clock signal. Since the phase of the parallel signal and the input data signal cannot be compared, the parallel signals are serialized to a serial data by the MUX according to the 1/K clock signal. The serial data is the above-mentioned decided data of which the phase is synchronized with the 1/K clock signal (VCO clock signal) and the bit sequence is the same as that of the input data signal. The phase of the output serial signal is then compared with the phase of the input data signal by the phase comparator.

Since the "Okamoto" reference does not identically describe (or even suggest) the above-discussed features of claims 1 and 18, the rejected independent claims are allowable, as are their respective dependent claims.

With respect to paragraph three (3) of the Office Action, claim 3 was rejected under 35 U.S.C. § 103(a) as unpatentable over the "Okamoto" reference.

With respect to paragraph four (4) of the Office Action, claim 4 was rejected under 35 U.S.C. § 103(a) as unpatentable over the "Okamoto" reference in view of Obana et al., U.S. Patent No. 5,001,711.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

As to claim 3, it depends from claim 1, and is therefore allowable for the same reasons as explained above as to claim 1 as to the "Okamoto" reference.

As to claim 4, it depends from claim 1, and is therefore allowable for essentially the same reasons as explained above as to claim 1 as to the primary "Okamoto" reference, since the secondary "Obana" reference does not cure the critical deficiencies of the primary "Okamoto" reference, as explained above. This is because any review of the secondary

"Obana" reference makes clear that it simply does not in any way disclose or suggest the claim 1 or claim 4 features, as explained above.

Accordingly, claims 3 and 4 are allowable.

It is therefore respectfully submitted that claims 1 to 7 and 12 to 18 are allowable – like allowed claims 8 to 11.

Conclusion

It is therefore respectfully submitted that all of claims 1 to 7 and 12 to 18 are allowable -- like allowed claims 8 to 11. It is therefore respectfully requested that the objections and rejections be withdrawn, since all issues raised have been addressed and obviated. An early and favorable action on the merits is therefore respectfully requested.

Respectfully submitted,

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